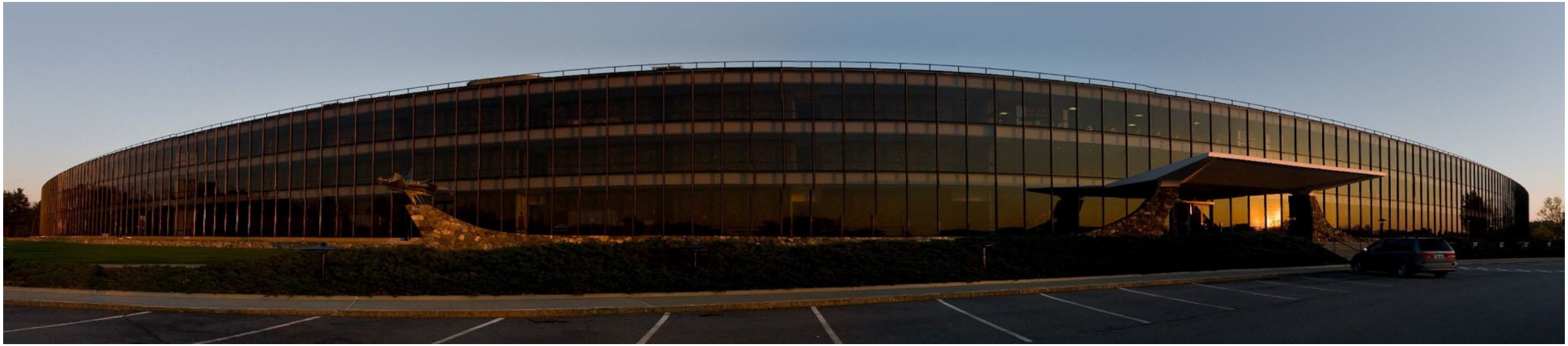
Lead by Dirk Pfeiffer (dirkp@us.ibm.com)



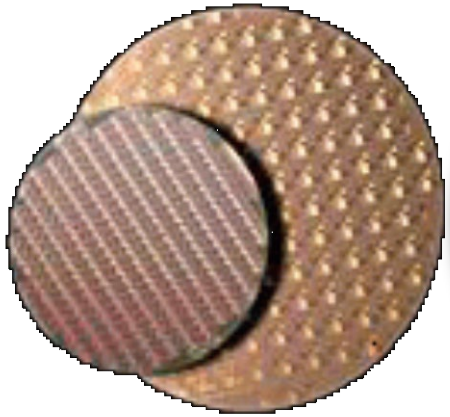
IBM Research Microelectronics Research Laboratory

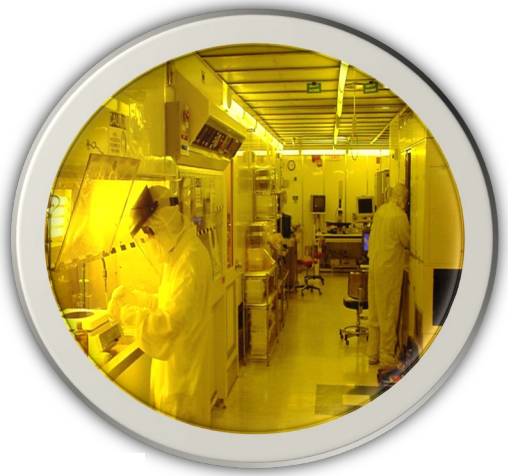
What is the MRL?

- A 200mm wafer-scale unit process development & advanced prototyping facility located in Yorktown
- 50K sf of clean room space, ~200 tools, dedicated staff (200 scientist and engineers)
- Rich history of semiconductor technology innovation (CMP, STI, HiK MG, technology scaling, Cu, SOI, FINFET, Nanowire, SiGe FIN…..)
- Range of capability for advanced prototyping, Standard CMOS flow + tools & Packaging
- Flexibility and operational discipline: new materials while yielding testable arrays

200/300mm lab to fab transition

- **Precompetitive development of new materials, devices, unit processes without 300mm process flow disruptions, collaboration with academia**
- **Transfer to 300mm via bridge tools (200/300mm capable), Unit process JDA with semiconductor vendors**
- **IBM commercially developed semiconductor knowhow also transferable to DoD**





IBM Research Lab to Fab Model

Process transfer to manufacturing partner

300mm Si wafer scale process development (EUV)

IBM NY Creates Albany Nanotech

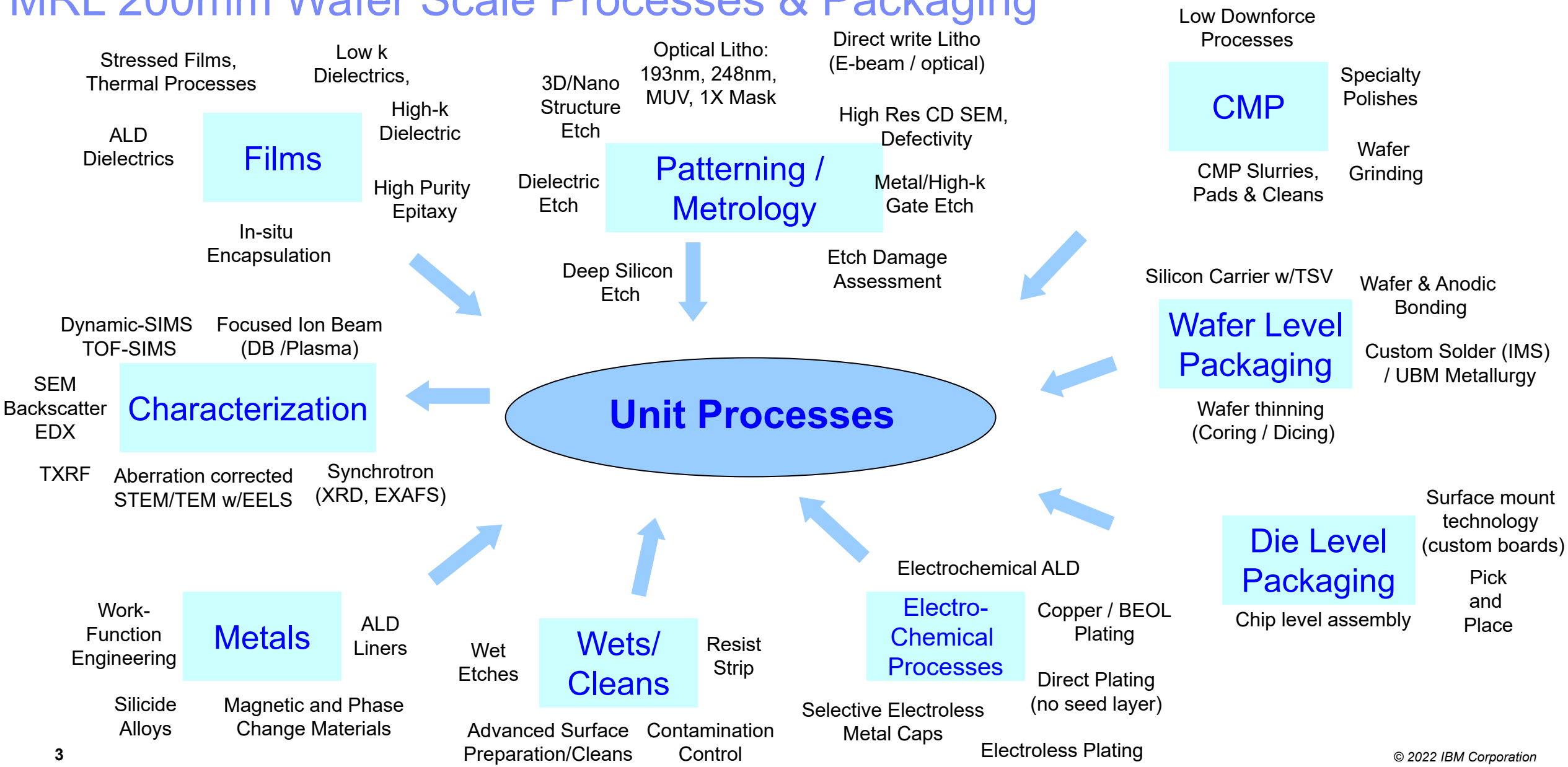
200mm Si wafer scale process development (ebeam & optical lithography)

IBM Yorktown Microelectronics Research Laboratory

Early device/package prototyping; Small scale fabrication on Silicon (ebeam lithography); new materials;

Nanofabrication Almaden, Zurich

MRL 200mm Wafer Scale Processes & Packaging



MRL MEC Offerings

Advanced Packaging Development

- Wafer, Module, Card and System Level Packaging Development
- Solutions for Power Management, Cooling, Chiplets, 3D/2.xD, High Density Interconnect, Bonding, Compression Molding
- Integration of Silicon and non Silicon

Die and wafer level Packaging capability within the MRL:

- Dicing - conventional, coring, beveling, notching, edge trim and stealth including 200/300mm wafer
- Bump Bonding - various solders, as small as 40 μm pitch
- Wire Bonding - auto, manual and ball (stud)
- Wafer Bonding - glass to silicon and silicon to silicon adhesive bonds, bond debond
- Electroplating Processing and Development – Ni, Cu, Au, Pd, Pt, Sn, In
- UBM Development - conventional and for new solder material
- Lithography – direct write, 0.5 μm resolution, planarizing high aspect ratio features
- Injection molded soldering, Unique TDV and TSV Etch Capability for HI Applications, Etch Process Solutions through thick BEOL

200mm wafer scale processing

- Unit process development of new devices and materials at 200mm wafer scale with standard CMOS tooling
- Process flows for integration of new devises and materials in BEOL on prefabricated foundry FEOL (90-180nm)
- Process modules for new FEOL/BEOL materials learning

MRL 200mm wafer scale processing capabilities:

- Optical lithography including 0.75NA 193nm, laser direct write and ebeam lithography for 200mm wafer scale device development
- Testable yielding arrays of analog devices integrated in BEOL fabricated on 90-180nm transistor arrays provided by foundry partner (split fab and wafer exchanges)
    - Devices include PCM, MRAM, RRAM and others
- FEOL and BEOL module based arrays for transistor level and interconnect learning of new materials and processes
- Unit process develop of new materials and processes including ALD, CVD, PVD, RIE, CMP, plating and other
- 200/300mm hybrid tooling for rapid transfer of process learning from 200 to 300mm