New York Center for Research, Economic Advancement, Technology, Engineering and Science

Albany 300mm Fab Facilities and Technology

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NYCREATES

NY CREATES

New York Center for Research, Economic Advancement, Technology, Engineering and Sciences

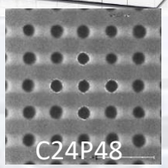
Mission	• NY CREATES accelerates next generation semiconductor technology research and develops the workforce to support the innovation economy
Infrastructure and Ecosystem	• 20+ year history of public-private R&D partnerships & investment • Capital investment in excess of $15 billion • 100k+ sq ft of 300mm cleanroom fabs – CSR, AMAT META, TEL TTCA
Partners	NYCREATES, IBM, TEL Tokyo Electron, Applied Materials, ASML, SCREEN, Lam Research, SUNY The State University of New York, and more
Technology Enablement	• Logic node range: 2nm nanosheet transistors → 65nm Photonics derivatives • Novel memory, neuromorphic computing, quantum computing • Heterogeneous Integration and Packaging
Engagement Models	• Development Agreement, Development Associates, Wafer Processing • Custom Fabrication, Test Evaluation, Product and Services Purchase

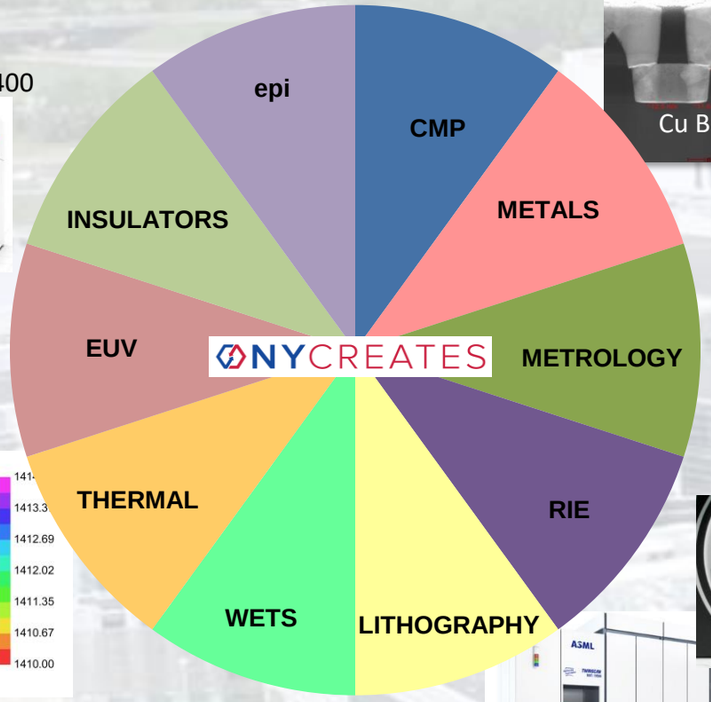
NYCREATES

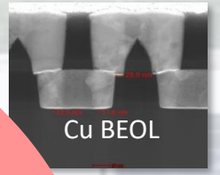
World-Class Capabilities at NY CREATES

300mm Si Fab Capabilities – Full-flow FEOL and BEOL

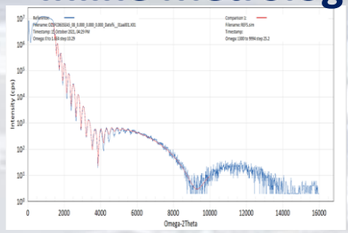
ASML TWINSCAN NXE:3400

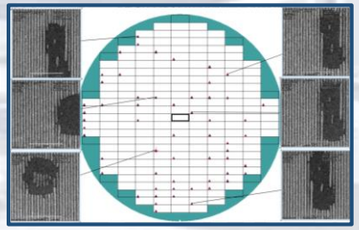


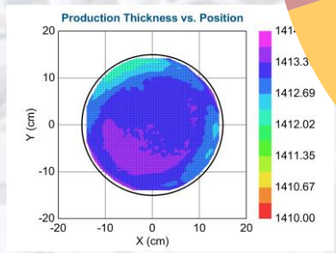


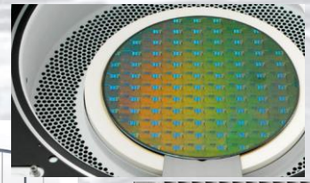


Inline Metrology and Defectivity

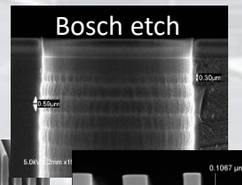


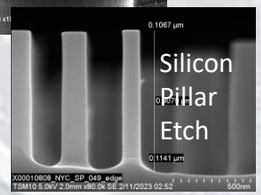




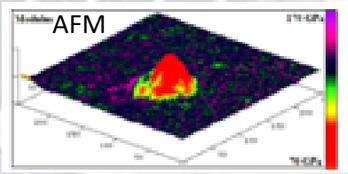


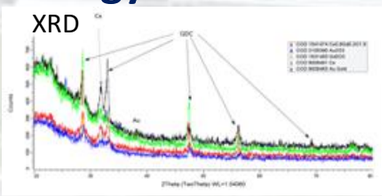
ASML TWINSCAN NXT:1950i



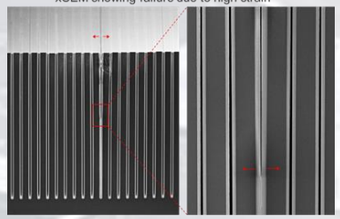


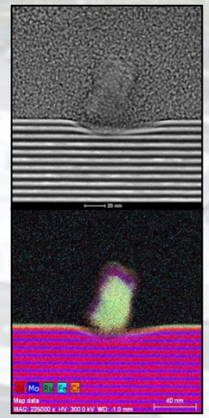
Offline Metrology





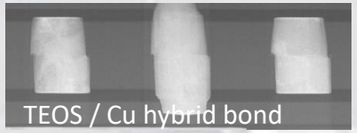
Failure Analysis

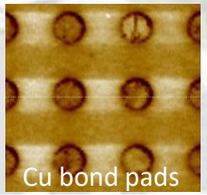


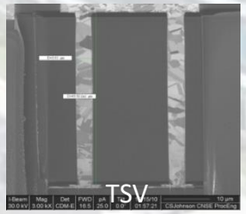


Heterogeneous Integration (HI) Fab Center

- Fusion Bond, Die-to-Wafer Bond, Temp Bond, Debond
- Post-bond Grind and Bond Test
- Bump Metallization
- TSV integration







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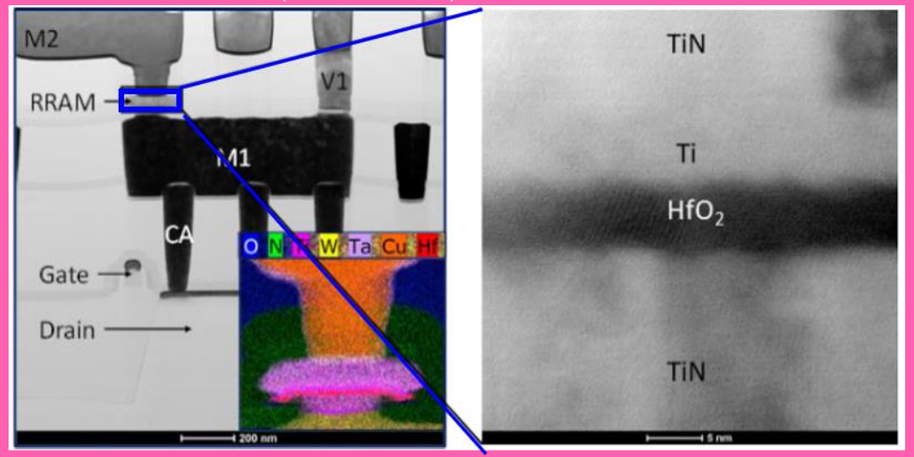
Technology Development at NY CREATES

ReRAM

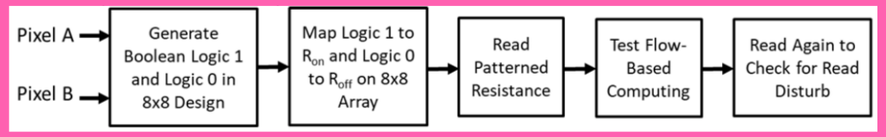
TEM of 1T1R integration of HfO_2 RRAM devices and inset of EDX compositional analysis of ReRAM stack



J. Hazra, M. Liehr, K. Beckmann, S. Rafiq and N. Cady
2020 IEEE International Integrated Reliability Workshop (IIRW)

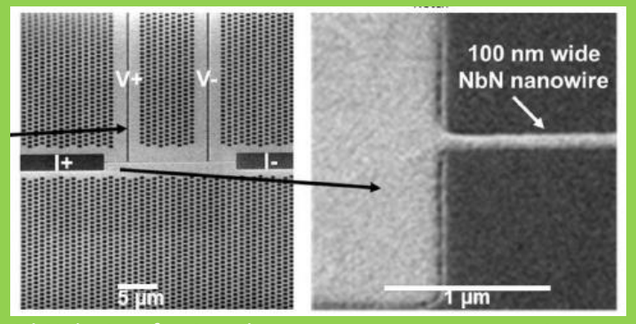
- CMOS/RRAM Hardware *In-memory Computing*
  - Used 8x8 1T1R arrays to perform flow-through computing for image pixel comparison / edge detection.
  - Bitwise comparison of pixels results in robust image edge detection in both simulation and experimentally on 1T1R arrays.

Pixel Comparison in 8x8 1T1R Array

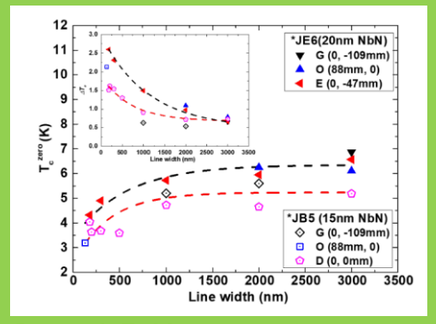


S. Rafiq, J. Hazra, M. Liehr, K. Beckmann, M. Abedin, J.S. Pannu, S.K. Jha, **N.C. Cady.**
Accepted - IEEE Transactions on Circuits and Systems – April 2021

Superconducting and Quantum Computing



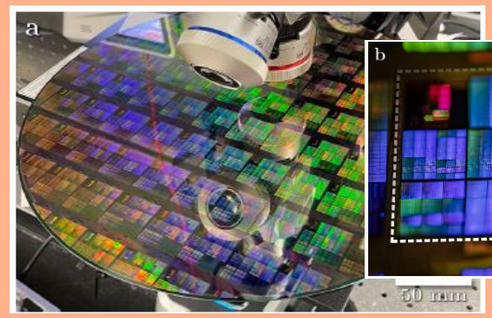
NbN devices for 4-probe measurement at cryogenic temperatures



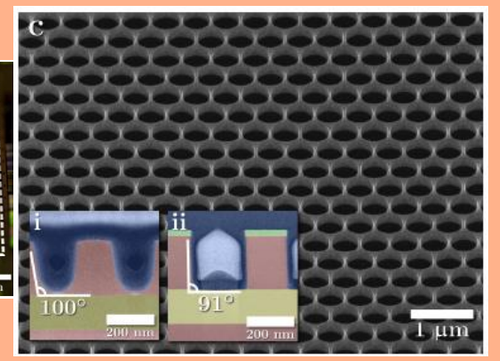
Cryogenic Tc Measurements

Soumen Kar, et. al., *TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, VOL. 33, NO. 5*, AUGUST 2023

Photonic Crystal Fabrication



Full-wafer photonic crystal fabrication in an optimized 300 mm foundry process. A wafer contains 64 complete reticles.



Millions of inverse designed PhC cavities. The before (i) and after (ii) false-color (blue: metal II; red: silicon; yellow: silicon dioxide; green: etch mask) transmission electron microscope cross-sections show how process optimization enables high-quality PhC lattices.

Christopher L. Panuski, ***Nat. Photon. 16, 834–842 (2022)***

THANK YOU

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